HERITAGE INSTITUTE OF TECHNOLOGY

TIME TABLE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING M.TECH VLSI

SESSION: 2021-2022

2nd YEAR, 1st SEMESTER

DAY	9.00 AM – 9.55AM	9.55 AM – 10.50 AM	10.50 NOON – 11.45 PM	11.45AM- 12.25PM	12.25 PM – 1.20PM	1.20PM – 2.15 PM	2.15 PM – 3.10 PM	3.10 PM – 4.05 PM	4.05PM- 5.00PM	5.00PM- 5.55PM
MON		L/MATH 6121/MS	L/MATH 6121/MS							
TUE						L/VLSI 6132/KM	L/VLSI 6132/KM			
WED			L/VLSI 6132/AMB	Break						
THU					L/VLSI 6125/SM					
FRI	L/VLSI 6125/SM	L/VLSI 6125/SM			L/MATH 6121/DC					

To be effective from 1st October, 2021 A minimum of 75% attendance is mandatory for being eligible to sit for the End-Semester Examination. Students should target 100% attendance

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TIME TABLE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING M.TECH VLSI

2nd YEAR, 1st SEMESTER

SESSION: 2021-2022

FACULTY NAMES

Faculty names	Initials	Department
Prof. Amrita Banerjee	AMB	ECE
Prof.(Dr.) Kasturi Mukherjee	KM	ECE
Prof.(Dr.) Susovan Mandal	SM	ECE
Prof.(Dr.) Dipankar Chakraborty	DC	Mathematics
Prof. Moulipriya Sarkar	MS	Mathematics

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING M.TECH VLSI

2nd YEAR, 1st SEMESTER

SESSION: 2021-2022

COURSE STRUCTURE

2nd, Year, Semester I

	A. Theory							
Sl. No.	Course Type	Code	Course Title	Contac	ct Hour	s/Wee	k	Credits
				L	T	P	Total]
1	Professional Elective PE-5	VLSI6131	Nano materials and Nano Technology	3	0	0	3	3
		VLSI6132	RF IC Design and MEMS					
2	Open	MATH6121	Optimization Techniques					
	Elective	CSEN6121	Business Analytics					
		ECEN 6125	Design and Technology for Photonic Integrated Circuit	3	0	0	3	3
		AEIE6123	Intelligent Control					
		Total of Th	eory	6	0	0	6	6

	B. Sessional							
1	Dissertation	VLSI6195	Dissertation Phase I	0	0	20	20	10
		Total of Se	mester	6	0	20	26	16

Open	ECEN6121	Ad Hoc Networks and Uses	3	0	0	3	3
Elective				1	1	l	1
	ECEN6122	Embedded Systems			l		
	ECEN6123	Cognitive Radios			l		
	ECEN6124	Automation in VLSI Design	\neg		1		1

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